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 PATENT & TRADEMARK OFFICE

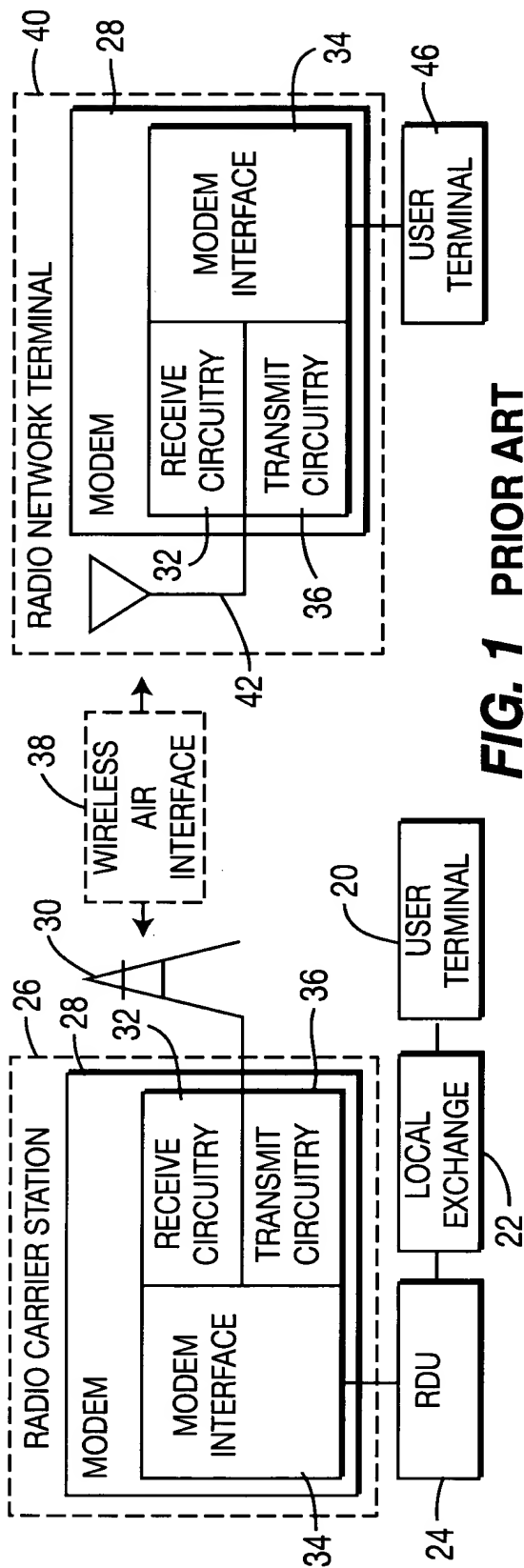


FIG. 1 PRIOR ART

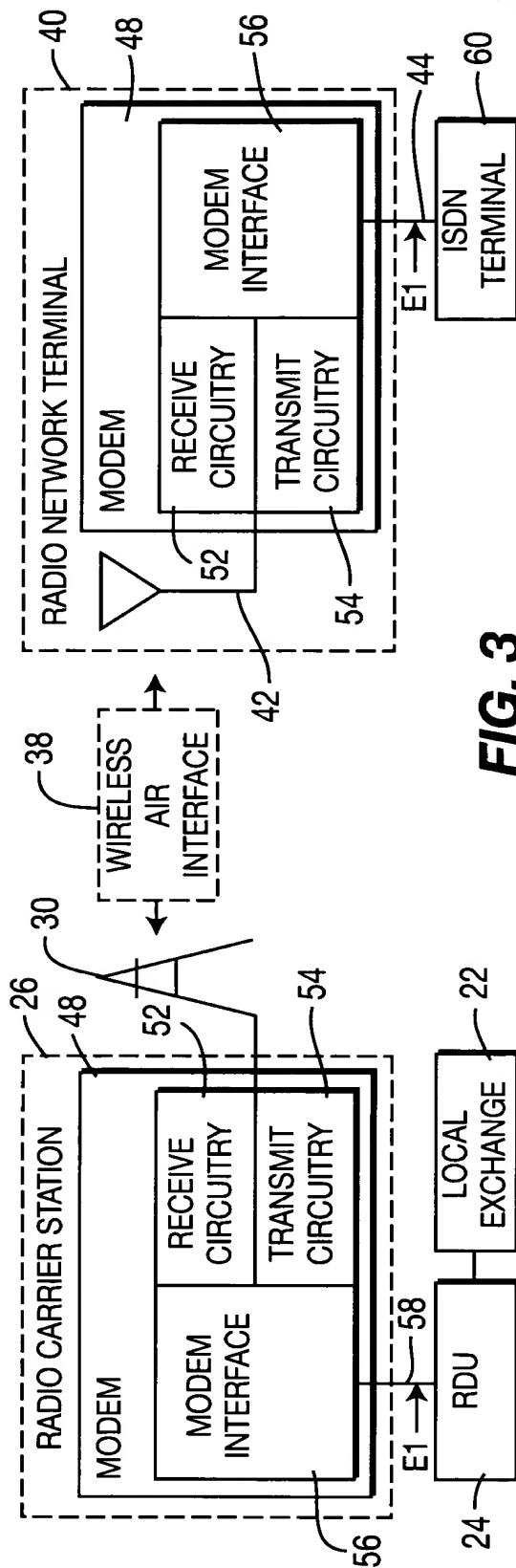


FIG. 3

**FIG. 2B**

Figure 1 is a block diagram of a multi-processor system architecture. The system includes a PCM HWY IN/OUT, PCM/IOM, I/O, ARM, API, DSP, HDLC 1-3, HMUX, IOM INTERRUPT, and various registers (BR, R, W). It shows connections to 9 HDLC SLOTS, 3 ARMSLOTS, 8 IOM SLOTS, 8 DSP SLOTS, and 3 INTERNAL PCM HWYS.

**FIG. 2A**



MODEM INTERFACE-TSI BLOCK

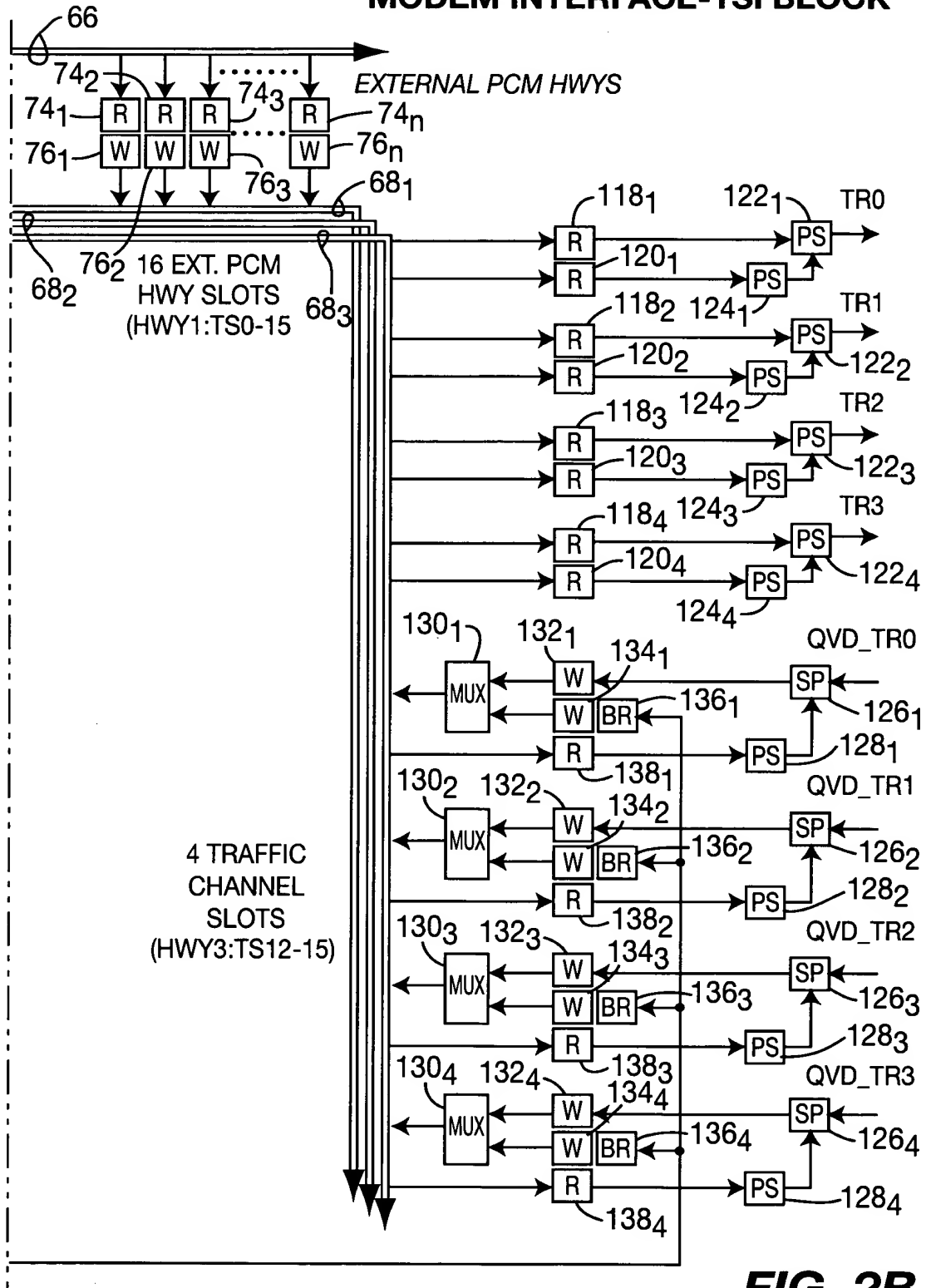


FIG. 2B